

AMENDMENTS

Please amend the above-identified application as follows:

In the Claims:

This listing of claims replaces all prior versions and listings of claims in the application.

1 1. (Currently Amended) An apparatus for performing the addition of a
2 propagate, kill, and generate recoded numbers, said apparatus comprising:
3 a circuitry configured to receive at least a first operand, ~~and~~ a second operand,
4 and a carry-in bit, the first and second operands comprising respective first and second
5 propagate, kill, and generate recoded number representations of respective first and
6 second binary operands;
7 a first carry-save adder configured to add said first operand and said second
8 operand to generate a third propagate, kill, and generate recoded number
9 representation and a carry-out bit; and
10 a modified carry-save adder configured to receive the third propagate, kill, and
11 generate recoded number representation from the first carry-save adder, the carry-out
12 bit, and the carry-in bit from the circuitry, add the separate propagate, kill, and
13 generate bits of the third propagate, kill, and generate recoded number representation
14 ~~in accordance~~ with a the carry-out bit and the carry-in bit to generate a sum value and
15 a carry value.

1 2. (Original) The apparatus of claim 1, wherein said sum value and said
2 carry value are dual rail encoded values.

1 3.-6. (Canceled)

1 7. (Currently Amended) A method for processing propagate, kill, and
2 generate representations of respective first and second binary operands, comprising:
1 receiving a carry-in value and a first and a second propagate, kill, and generate
2 representation of respective first and second binary operands;
3 adding the first and second propagate, kill, and generate representations to
4 generate a third propagate, kill, and generate representation and a carry-out value; and
5 mathematically combining the third propagate, kill, and generate
6 representation ~~in accordance~~ with the carry-out value and the carry-in value to
7 generate a sum value and a carry value.

1 8. (Previously Presented) The method of claim 7, wherein said step of
2 mathematically combining comprises adding the third propagate, kill, and generate
3 representation and the carry-in value.

1 9. (Canceled)

1 10. (Previously Presented) The method of claim 7, wherein said step of
2 mathematically combining further comprises generating dual rail encoded values.

1 11-22. (Canceled)